FPGA-Based Control System of an Ultrasonic Phased Array

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One of the main features of ultrasonic phased arrays is the ability to create an ultrasonic focused beam by applying time-delayed signals to each one of the elements of the array. If the focused beam can sweep a certain area it is possible to obtain a B-scan image. This process is called beamforming.

In this work, a prototype control system for a phased array, based in a FPGA (Field Programmable Gate Array), was conceived. The array has 30 elements and is to be used in B-scan low resolution imaging (50×50 pixels). Time-delayed was implemented by means of a 50 MHz oscillator, which allows a minimum delay of 20 ns. By using nine bits counters it is possible to obtain a maximum delay of 10.24 μs between control signals. The scanning sector area is 60 mm in depth and a ±30° aperture.

0 INTRODUCTION

The ultrasonic waves are mechanical vibrations that can propagate through many different types of materials. Typically, in ultrasonic non-destructive testing (UNDT), an ultrasonic signal is transmitted into the material to be tested, after which this signal is collected and processed to obtain information that may be related to parameters or properties of that material. A classic application is the detection of defects or inclusions inside a given material: the ultrasounds when travelling between materials with different properties (interface material/ defect), give rise to a reflected wave, which can be used for identification and classification of defects or inclusions. After a defect has been located in a given material it is often important to have information about their shape and size and then make decisions about its integrity. In the medical field, 2D US images are an important means of diagnosis essential to evaluate many clinical situations.

One of the most often used techniques is the ultrasonic B-scan imaging. This technique combines the information obtained by a one-dimensional A-scan method, related to the ultrasonic beam propagation inside the material, with a mechanical movement that produced an image parallel to the direction of propagation. The time-of-flight (travel time) of the sound energy is displayed along the vertical axis and the linear position of the transducer is displayed along the horizontal axis. The mechanical movement made by the transducer is usually replaced by an electronic scanning of the beam, by means of a phased array [1] and [2]. In the most basic sense, a phased array system utilizes the wave physics principle of phasing. Varying the time between a series of outgoing ultrasonic pulses in such a way that the individual wave fronts generated by each element in the array combine with each other to add or cancel energy in predictable ways that effectively steer and shape the sound beam.

In the last decades there has been considerable advancement in the ultrasound systems function and their beamformers [3]. The first techniques used to implement the delays among the different elements of an array were based in analog systems like lumped elements, electromagnetic delay lines or charge transfer devices [4]. In modern ultrasound scanners a wide variety of beamforming approaches are applied using digital processing. Some of them use classical full phased array imaging and sweep out a sector image by beam steering across the image space, where all elements are active during both transmission and receiving [1]. Other developed techniques use a different number of active channels and different approaches: parallel receiving phase rotation [5], single-bit delta-sigma conversion [6], direct sampled in-phase/quadrature

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beamformer [7] or phased subarray imaging [8]. Also, FPGA based systems have been developed where power dissipation [9] and compact size [10] are important project parameters.

In this work, a way to implement the delays to be provided to each of the elements of a linear array with 30 elements, designed to obtain low resolution ultrasonic B-scan images is presented. In the proposed implementation a low cost and high scale of integration solution, based on an FPGA xc3s1000 from Xilinx, was used.

1 ULTRASONIC B-SCAN IMAGING WITH PHASED ARRAYS

In most conventional ultrasonic inspections only one probe is used and the information gathered is related to propagation axis. If this monoblock probe is divided into several elements (array) with width much less than its length, we can assume that each of the elements leads to a linear source of cylindrical waves. The wave fronts of the array elements will interfere, generating an overall wave front [11]. The new wave fronts may be delayed and synchronized with each other in terms of phase and amplitude in order to create an ultrasonic beam with the possibility of focusing and steering. The individual control of each of the elements of the array is made to give rise to a focused beam, with the possibility of changing some parameters such as angle, the focal length or size. This process is controlled by dynamic software. The scanning of the focused beam allows detection of defects with several orientations, as well as outside of the propagation axis. These situations are illustrated in Fig. 1a: a single probe showing some limitations in the detection of defects presenting the illustrated orientations or located outside the propagation axis.

To produce a beam with constructive interference, the various elements of the array must be excited with signals with small time differences between them. Fig. 2 shows the acquisition and control system for the transmitted (a) and received signals (b), in order to produce a focus on the desired point. The collected signals are shifted in time, as shown in Fig. 3 before being added. The result is an A-scan signal that emphasizes the response of the desired focal point and attenuates the echoes from other points of the testing material.

During the transmission, the acquisition unit sends a trigger signal to the control system, which converts this signal into a high voltage pulse with a time delay and width programmed according to the focal law. Each element receives only one pulse, giving rise to a beam with a specific angle and focal length. When the beam reaches the defect a reflection occur and the signal is collected by each one of the elements of the array, and time-shifted according to the parameters of the system. Finally, the signals are combined so that only one ultrasonic pulse is delivered to the acquisition system. Fig. 4 shows the beam focusing for an angled incidence.

There are several techniques of beam scanning to obtain an image [8]. Typically, in phased arrays with a high number of elements, a sequential excitation of a group of active transducers with the same delay is done along the array. In other cases, it may be a scan based on changes in focal length, with all elements to be used simultaneously and focalization on the receiving stage. Other techniques use a
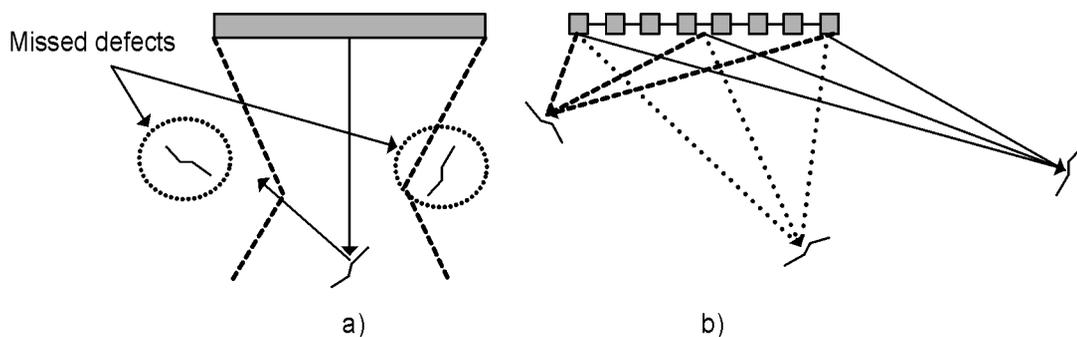
Fig. 1. *Detection of misoriented defects by: a) monocrystal probe; b) multielement probe*

focalization of all elements simultaneously with constant distance from the centre of the array and variable inclination.
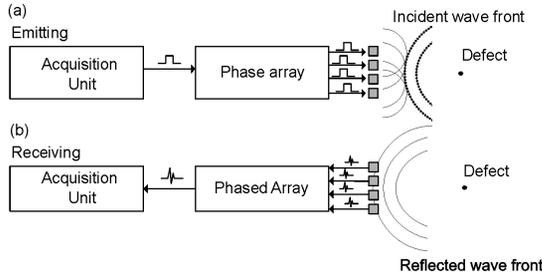
Fig. 2. *Acquisition and control system of the phased array: a) transmission; b) reception*
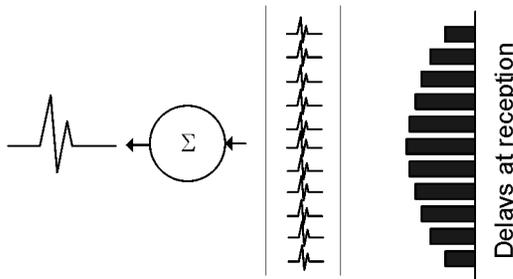
Fig. 3. *Delays in the reception*
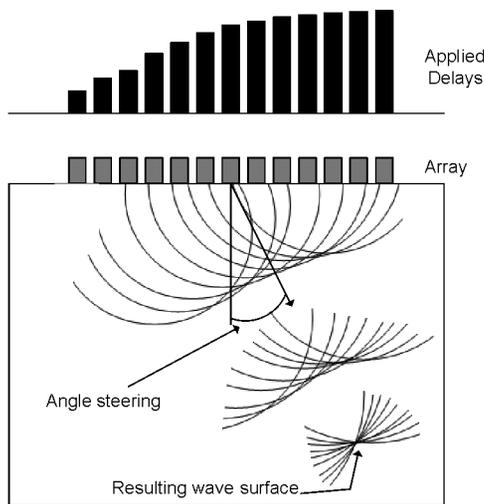
Fig. 4. *Beam focusing for angled incidence*

2 FOCUSING DELAY CALCULATION

To make the focusing of a phased array transmitted beam at a particular point, it is assumed that each of its elements will behave as a point source and the radiation diagram is omnidirectional in the plane of interest. For a homogeneous medium with constant wave speed, it is then necessary to determine the distances from each one element of the array to the focussing points. The resulting delays are obtained from the corresponding ratio between the distances and wave speed in the medium.

Fig. 5 depicts the geometry used to deduce the expression for calculating the delays to provide to a phased array with an even number of elements.
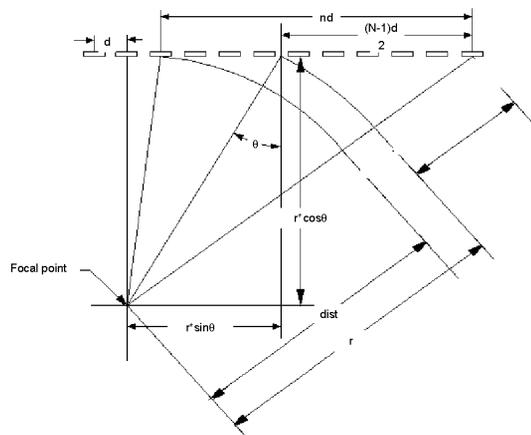
Fig. 5. *Geometry of a linear phased array used to deriving the focusing formula*

For a particular focalization point with polar coordinates (r, θ), it is possible to obtain the distances $(dist_n)$ to each array element by the expression:

$$dist_n = \sqrt{(r\cos\theta)^2 + (r\sin\theta + (\frac{N-1}{2} - n)d)^2} , \qquad (1)$$

where:
r is the distance to the centre of the array [m],
N is the number of elements of the array,
n is the index of the array element,
d is the distance between two consecutive elements [m].

Using an auxiliary variable defined as k_n

$$k_n = (\frac{N-1}{2} - n)d , \qquad (2)$$

the Eq. (1) can be simplified leading to:

$$dist_n = \sqrt{r^2 + 2k_n r \sin\theta + k_n^2} \ . \qquad (3)$$

The delays can now be calculated by:

$$delay_n = \frac{dist_{max} - dist_n}{c} \ , \qquad (4)$$

where c is the wave speed in the medium [m/s], $dist_{max}$ is the maximum distance value [m].

With the present system, we intend to control an array with 30 elements having 1 mm separation between elements, capable to produce a scanning area from 10 to 60 mm in depth with an aperture of ±30º. Fig. 6 shows schematically these dimensions. The low resolution image has 2500 pixels (50×50), corresponding to 1 pixel/mm in the direction perpendicular to the array (depth) and a minimum of 1.35 pixel/mm in the angle direction.
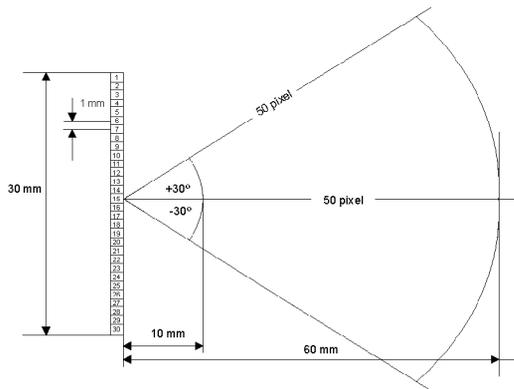
Fig. 6. *Scanning area*

The situation where there are major differences between the delays is for the closer points to the array. For the minimum focalization distance (10 mm), the maximum delay between the central element and one of the extremes of the array can be easily calculated, and for the present case is 5.3 µs.

The delays are implemented based on synchronous counters which operate at a frequency of 50 MHz, allowing a minimum counting period (delay) of 20 ns. As it will be used 9 bit counters, maximum delay values of $2^9 \times 20$ ns $= 512 \times 20$ ns $= 10.24$ µs are possible, which is about two times above the desired specifications.

3 DELAY IMPLEMENTATION

The implementation of the delays was done using a Xilinx FPGA xc3s1000 from Spartan-3 family. The Digilent programmable logic board presented in Fig. 7 and VHDL programming language were used for that goal. This board has high-speed USB2 port, together with a collection of I/O devices (VGA output, push-buttons, switches and LCD display), data ports and expansion connectors that allow a wide range of designs to be completed without needing any additional components.

The simplified block diagram of hardware implementation is depicted in Fig. 8. Each block represents a programming module and is controlled by the whole global program responsible for data loading.
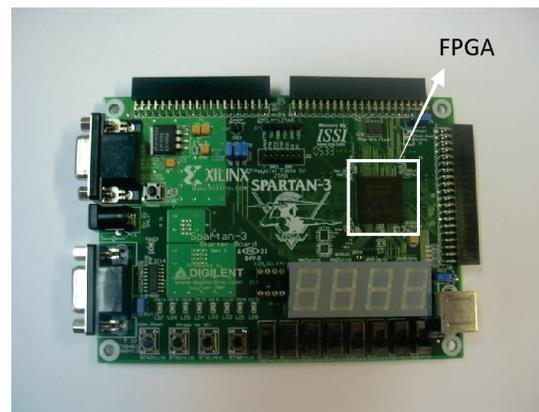
Fig. 7. *Programmable logic board*

The *Calc_sin* module provides the sin values of the angle corresponding to the focalization point, relatively to the centre of the array. As VHDL language does not support the *sin* function, a solution often used in programmable devices that consists of the creation of a *lookup table* (LUT) with the 50 values was implemented, corresponding to the 50 points of the angular scanning (±30º).

To determine different distances from the focalization points to the elements of the array, the Eq. (3) will be used with the parameters n, d and N previously defined. Again the strategy of calculating the square root needs to be used as this is not supported by the language. In this

case the use of LUT is not adequate because it would consume many resources (50×50 values), so the alternative was the development of Eq. (3) in terms of Taylor series. This module is called *Calc_dist*. After calculating the distances, the module *Calc_dist$_{max}$* determines the maximum of all distances.
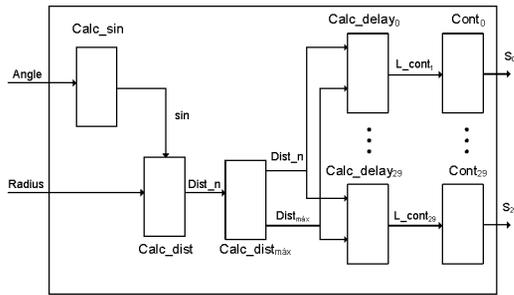
Fig. 8. *Simplified block diagram of the array control system*

From this point, the system will have as many parallel channels as the number of elements of the array, which is 30 for the present system. From the set of distances previously calculated and using its maximum value, the delays will be calculated using the module *Calc_delay_n*, which in practice implements the Eq. (4). After the calculation of the delays, these values must be converted to multiples of the time unit of the system, which are 20 ns. As already mentioned, the system uses 9 bit counters, which allows a maximum number of 512 counts. The initial value to load each one counters, *L_cont$_n$*, is then given by:

$$L\_cont_n = 512 - \frac{delay_n}{20}, \qquad (5)$$

where: *delay$_n$* is delay of nth element [ns].

The greater the value of *delay$_n$*, which indicates a higher proximity of the element to the focalization point, the lower the *L_cont$_n$* value to provide to the counter.

The final module *Cont$_n$* consists of a counter. After all *L_cont$_n$* signals have been loaded, a control signal sent to all counters (not represented) will start the count of each one from the original value *L_cont$_n$*. The control signals of the array *S$_n$* will change its state when each a

counter reaches the maximum count, leading to the desired shift to provide to the corresponding element.

For a new focalization point, the whole process is repeated, with the introduction of the angle and radius parameters.

4 RESULTS

At this stage the system was only tested for a focalization in a single point. Fig. 9 shows the timing diagram for the outputs S_n corresponding to a focalization point with an angle of +9° and a distance of 43.5 mm from the centre of the array. As can be seen, the shifting between the signals agrees with the predictions: the transducers further away from the focalization point are excited first (extremes of the array) and the closest are excited later (centre of the array). Note that in this case, the excitation of the elements 12 to 16 is simultaneous, which is due to the fact that the spatial difference between them is very small, causing differences in the propagation times less than 20 ns. Delays were measured and found in accordance with the theoretical values given by Eq. (4).

It was also possible to verify that only 40% of all resources (10^6 gates) of the FPGA have been used. Thus, this circuit can be used in situations where controlling of larger number of elements or analyzing of greater scanning areas are needed. These results can be seen as an improvement when compared with the ones provided by other authors [9] and [10].

5 CONCLUSIONS

In this work, a way to implement a phased array control to be used in low resolution ultrasonic B-scan imaging has been developed. Using a FPGA, the signals were successfully obtained to excite the array elements. The experimental results are in agreement with the analytical calculations.

One of the major advantages of the presented implementation is the great degree of miniaturization when compared with the use of conventional electronic circuits. The used FPGA occupies an area less than 3 cm². It is also very versatile as the control system can be housed in

one standard FPGA that can easily be programmed and upgraded. Another advantage is related to the huge cost savings, because a simple laptop can be used to visualize the information.

The developed hardware allows controlling the array transmission. Future work will deal with developments concerning the reception of the collected signals and their processing, towards the formation of B-scan image of the interior of structures to be inspected.

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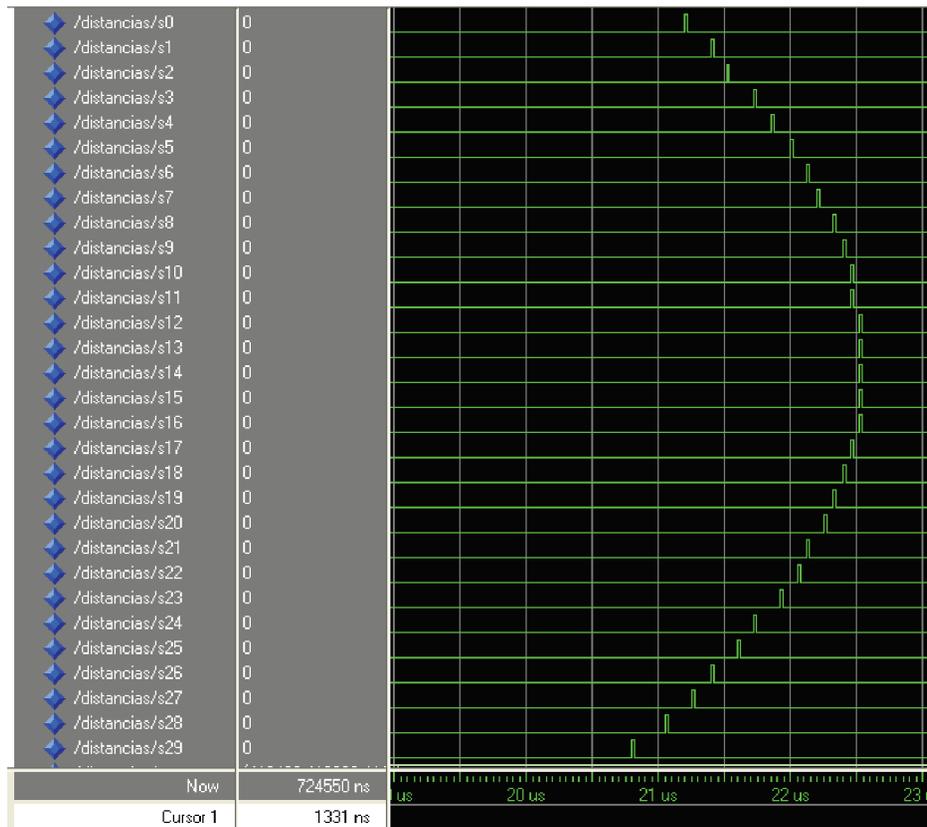
Fig. 8. *Timing diagram of the excitation signals for a focalization point with 9° inclination and 43.5 mm of distance, for the centre of the array*

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