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Integrirano oblikovanje izdelkov s področja drobnih elektromehanskih izdelkov

Integrated Design of Mycro-Electro-Mechanical Systems

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Ta prispevek želi najprej opredeliti postopek oblikovanja s področja izdelkov drobnih elektromehanskih sistemov. V tem delu želimo prikazati, kako nasloviti izdelovalnost. Le-to vsebuje znanje izdelovalnih postopkov, ki vodijo do izvedbe teh izdelkov (osredotočili se bomo na izdelke predvsem iz elektronske industrije). Nato si bomo ogledali glavne vrste metodologij oblikovanja, da bi razumeli, kako lahko upoštevamo izdelovalne tehnologije obenem pa so predstavljena še računalniško podprta orodja za te metodologije. Končujemo pri potrebah specifikacij za metodologije oblikovanja, ki bi ponudile oblikovalcem večjo neodvisnost od proizvodnih omejitev.

(Ključne besede: MEMS, DFM, omejitve proizvodne, metodologije oblikovanja)

This paper is a first attempt to qualify the design process in the field of micro-electro-mechanical systems products. Through this study we try to analyse how the issue of manufacturability is addressed. This requires an understanding of the specificities of the manufacturing process involved in the realization of these products (we focus on a process derived from the electronics industry). Then we look at the main design methodologies to understand how the manufacturing can be taken into account. Computer-aided tools associated to these methodologies are presented at the same time. Finally, we conclude on the need for specifications for the design methodology that would provide designers with greater independence from manufacturing constraints.

(Keywords: MEMS, DFM, manufacturing constraints, design methodology)

0 INTRODUCTION

MEMS (micro-electro-mechanical systems) are small components built of both electronic and mechanical parts. Their sizes (whole or part) range from a few micrometers to millimetres. A detailed taxonomy of microproducts can be found in [1]. A few MEMS are already integrated in mass-market products (automotive, cellular phones, ink-jet printers, PDA, etc.) but major potential applications are still to come.

MEMS are fundamentally multidisciplinary devices, and so are the design teams. Hence, designers from different disciplines need to communicate efficiently, but also have to collaborate with manufacturing experts. This last point is all the more important since micro-manufacturing processes are often unfamiliar to the designer in charge of the mechanical part. This lack of knowledge combined with the R&D context involves, most of the time, a traditional design approach for new products, based on "top-down" methodologies. This approach does not support collaborative design and implies many "build and test" iterations, which increase the time to market and product costs. In this paper we will try to describe design methodologies that are advocated to deal efficiently with the problem of manufacturability.

The next section is dedicated to a brief overview of the most representative manufacturing processes in order to have a better knowledge of what kind of constraints the designers have to deal with.

1 MEMS MANUFACTURING PROCESSES

The main manufacturing processes used in the micromachining of MEMS are derived from the silicon industry, with all electronic and mechanical parts being realized at the same time. Indeed, processes must be compatible with Very Large Scale Integration (VLSI) technologies: for instance, during the manufacturing sequence, the temperature should not exceed a certain value to avoid any alteration of the electronic parts. In general, a multiphysics as-

pect with strong coupling at this scale level will greatly influence the design process [2].

MEMS are built from silicon wafers by a sequential process consisting of stacking up layers of materials with appropriate geometries. Thus, the third dimension is not achieved in one step, but results from the whole sequence. The manufacturing operations are based on whether chemical or physical principles applied to the wafers. They can be broadly divided into three main processes, which are: additive processes, selective processes and etching processes. Patterns are created on the surface, or in the bulk, of the silicon wafer by selecting thin films previously deposed, and then etching processes remove material that has been selected. The organization of these three processes constitutes a step of the global manufacturing process, and one of the difficulties in MEMS manufacturing is to organize these steps in a manufacturing sequence. Indeed, processes used in a step should not deteriorate the material previously that is deposed, selected and etched.

1.1 Additive processes

The first building block in MEMS processing is the addition of thin films of material with a thickness between a few nanometres and about 100 micrometers. Additive technologies can be classified into two groups: addition that happen because of a chemical reaction or addition that happen because of a physical reaction.

1.1.1 Chemical Reaction

These processes exploit the creation of solid materials directly from chemical reactions in gas and/or liquid compositions or with the substrate material. The main processes are chemical vapour deposition, electrodeposition, epitaxy and thermal oxidation.

Chemical Vapour Deposition (CVD) The substrate is placed inside a reactor to which a number of gases are supplied. A chemical reaction takes place between the source gases and produces a solid material with condenses on all surfaces inside the reactor, including the substrate. The two most important CVD technologies in MEMS are:

Low-Pressure CVD produces layers with excellent uniformity of thickness and material characteristics and deposits films on both sides of at least 25 wafers at a time, but the deposition temperature is higher than 600°C.

Plasma-Enhanced CVD can operate at lower temperatures (down to 300°C), but the quality of the films tends to be inferior to LPCVD processes. Moreover, most PECVD processes can only deposit the material on one side of the wafers, at 1 to 4 wafers at a time.

A variety of materials can be deposited with CVD technologies; however, some of them are less popular with fabs because of hazardous the by products formed during the chemical reaction (Figure 1)

Example : Thick and smooth amorphous Si film of 2 μm without hillocks was obtained at a low temperature of 300°C by PECVD technology [3]. Fabrication of a suspended MEMS microstructure is thus possible (Figure 2)

Electrodeposition. The substrate is placed in a liquid solution (electrolyte) and requires an electrical potential to provide a chemical redox resulting in the formation of a layer of material on the substrate. This process is typically restricted to electrically conductive materials and it is well suited for making films of metal, such as gold, copper and nickel. The films can be made in any thickness from ~1μm to >100μm.

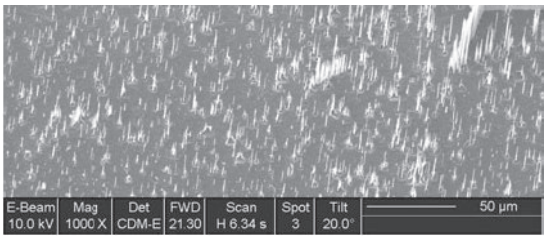

Fig. 1. *Example of bi-product "grass" formed by CVD process*

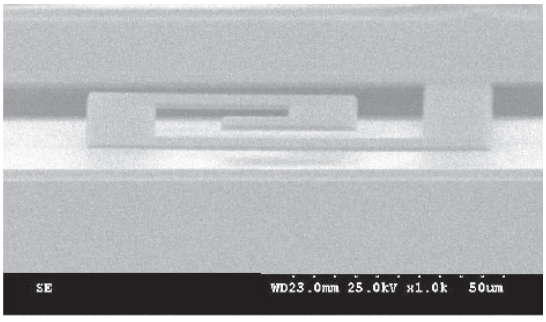

Fig. 2. *Suspended Si microstructure*

Epitaxy. If the substrate is an ordered semiconductor crystal (i.e., silicon, gallium, arsenide), it is possible with this process to continue building on the substrate with the same crystallographic orientation with the substrate acting as a seed for the deposition. An advantage of this process is the high growth of material, which allows the formation of films with a thickness of ~1µm up to 100µm. However, the temperature of the substrate must typically be at least 50% of the melting point of the material to be added. This technology is widely used for producing silicon on insulator (SOI) substrates.

Thermal oxidation. This most basic additive process simply involves oxidation of the substrate in an oxygen-rich atmosphere. This process is naturally limited to materials that can be oxidized and can only form films that are oxides of that material. The temperature is raised to 800–1100°C to speed up the oxidation.

1.1.2 Physical reaction

A common feature of all these processes is that the deposited material is physically moved on to the substrate. In other words, there is no chemical reaction that forms the material on the substrate. The main processes are physical vapour deposition and casting.

Physical Vapour Deposition. PVD covers a number of technologies in which the material is released from a source and transferred onto the substrate. The major physical principle called on is evaporation: the source material is heated to the point where it starts to boil and evaporate before deposing on the substrate. Many materials are restricted in terms of which evaporation method can be used. This typically relates to the phase-transition properties of that material.

Casting. In this process the material previously dissolved in liquid form in a solvent can be deposited on to the substrate by spraying or spinning. Once the solvent is evaporated, a thin film of the material remains. This is particularly useful for polymer materials (i.e., photo-resist), which may be easily dissolved in organic solvents, The thicknesses that can be cast on a substrate range all the way from a single monolayer of molecules (adhesion promotion) to tens of micrometers. The control of the film's thickness depends on the exact conditions, but can be sustained within ±10% in a wide range.

1.2 Selective Process

In the MEMS context the basic selective process is lithography, i.e., the transfer of a pattern to a photosensitive material (mainly photo-resist) by selective exposure to a radiation source such as light using a set of masks. The photo-resist can be either positive or negative; it then reproduces the pattern or its complementary image. Once the photo-resist is exposed it is developed, the pattern appears on the wafer, and the steps of the deposition or the

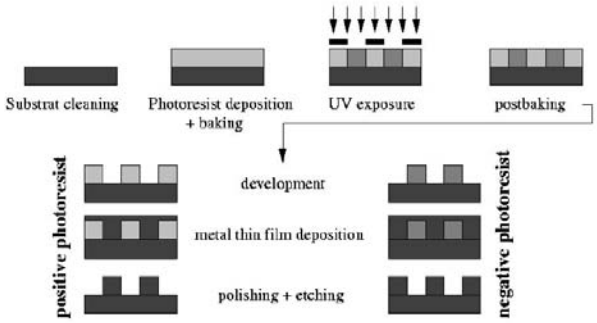

Fig. 3. *Photolithography and metal-deposition process steps*

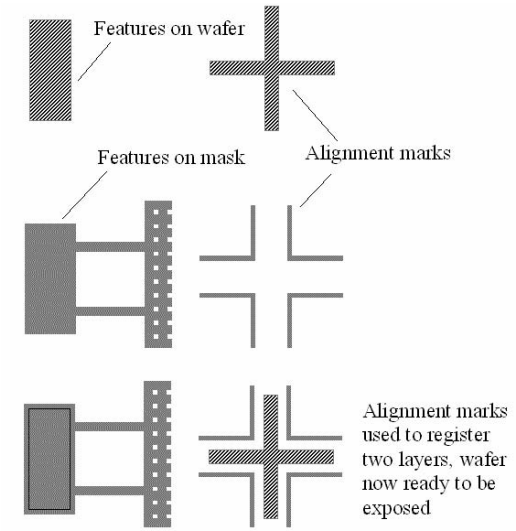

Fig. 4. *Use of alignment marks to register the subsequent layers*

etching then occur. A description of positive and negative lithography, metal deposition and etching is shown in Figure 3.

The main problem during this step is masks' alignment: the patterns for different lithography steps that belong to a single structure must be aligned with each other. The first patterns transferred to a wafer usually includes a set of alignment marks (Figure 4), which are high precision features. They stand as a reference for positioning subsequent patterns with respect to the first pattern.

Other problems, like the exposure parameters required to transfer an accurate pattern on to the photo-resist or the adhesion of the photo-resist on the substrate may occur.

1.3 Etching processes

Etching is the basic manufacturing step to remove material that has been selected during lithography in order to form a functional MEMS structure on the substrate. In general, there are four classes of etching processes. Wet etching, where the material is dissolved when immersed in a chemical solution; dry etching, where the material is sputtered or dissolved using reactive ions or vapour-phase etchant. These two etching processes being either isotropic or anisotropic. Anisotropic etching, in contrast to isotropic etching, means different etching rates in different directions in the material.

Wet etching. This is the simplest technology because all it requires is a container with a liquid solution that will dissolve the material to be removed. But a mask is desired to selectively etch the material, and one must find a mask that will not dissolve, or dissolve much more slowly than the material to be patterned. Etching a hole in a <100> silicon wafer in a chemical (such as potassium hydroxide, KOH) is an anisotropic etching process: the <111> crystal plane appear and the result is a pyramid-shaped hole.

Example: modelling and fabrication of the step-height control of a multilevel Si <100> structure in a KOH solution, using one photo-mask. Conventional multilevel structures are fabricated by lithography, deposition and etching technologies. Multi-masks are required for the multilevel structure formation: m masks can form (m+1) to 2^m level terraced structures. The plurality of masks and process cycles for film deposition, lithography and etching not only make the fabrication of a multilevel structure a long process with a high cost, but it also means that the misalignment problem of the masks cannot be avoided, as we have seen before. In [4] the authors propose a novel model for the step-height control of the Si <100> multilevel structure using one photo-mask and the KOH wet-etching process. The relationship between the step height and the widths and intervals of the masked areas was derived and experimentally verified. Figure 5 shows the mask pattern and cross-sectional diagram of a three-level terraced structure (a) and the micrograph after KOH etching (b).

Dry etching. These technologies can be split into several separate classes, one of which is reactive ion etching (RIE). In RIE the substrate is placed inside a reactor in which several gases are introduced. A plasma is struck in the gas mixture using an RF power source, breaking the gas molecules into ions. The ions are accelerated towards, and reacts at, the surface of the material being etched, forming another gaseous material by chemical reaction. If the ions have high enough energy, they can knock atoms out of the material to be etched without a chemical reaction. By

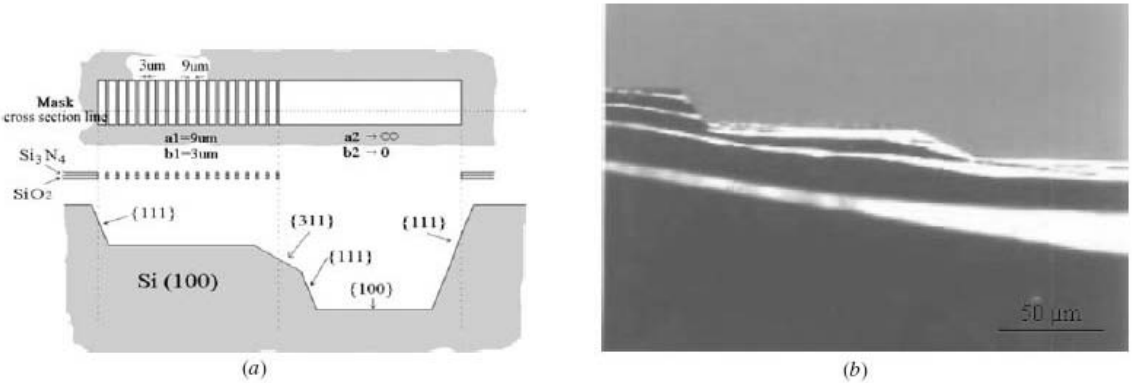

Fig. 5. *A three-level terraced structure with different step heights*

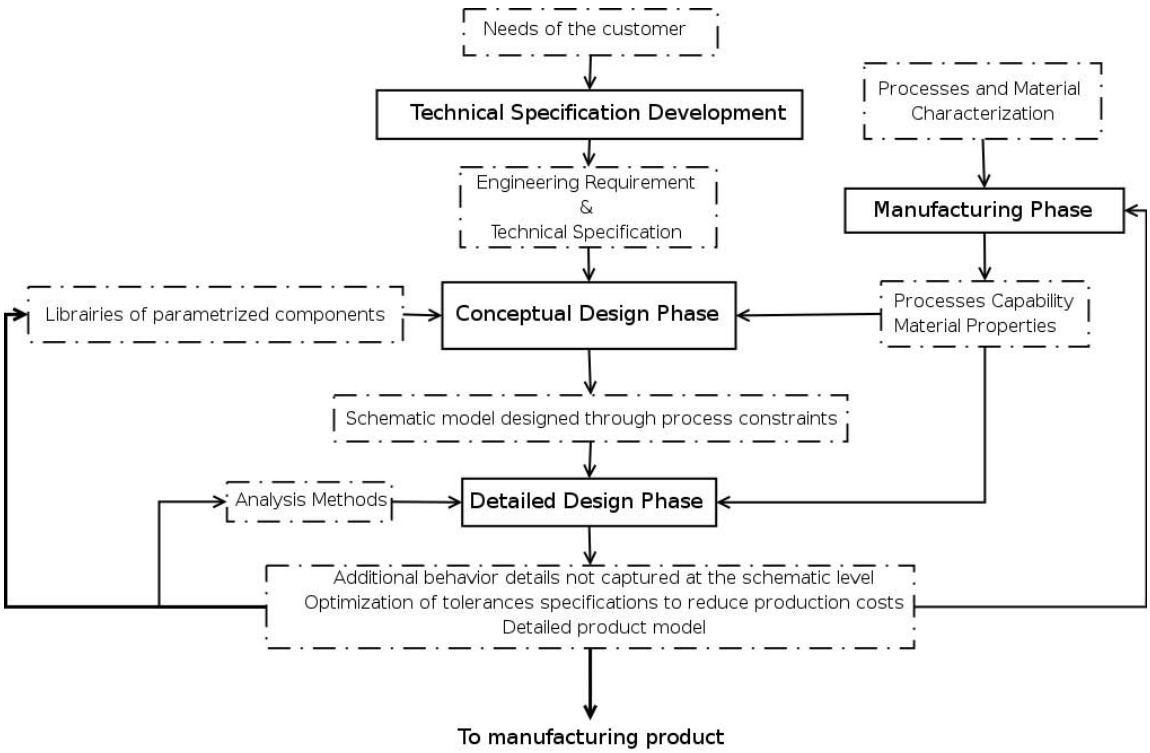

Fig. 6. *Schematic of DFM methodology implementation*

changing the balance between the chemical and physical reactions it is possible to influence the anisotropy of the etching, since the chemical part is isotropic and the physical part highly anisotropic the combination can form sidewalls that have shapes from rounded to vertical. A special popular subclass of RIE processes is Deep RIE (DRIE). This process can achieve depths of hundreds of microns with almost vertical sidewalls and an etching aspect ratio of 50:1. It can also be used to etch completely through a silicon substrate, and the etch rates are 3-4 times higher than wet etching. However, the cost per wafer, for a silicon wafer, will be 1-2 orders of magnitude higher than the wet etching. We have seen that it is possible to identify some process constraints and capability. Thus, the shape and the quality of the product depend on the selected process, since it influences: the quality (thickness and uniformity) of the deposited materials, the deposition rate, the formation of bi-products, the etched shape of the product, the electrical isolation of the wafer, the product costs, etc. We can also see that some parameters are few or less relevant in the choice of process. For example, the batch size is not as sensitive as in traditional macro-manufacturing because of the natural manufacturing organization in the batch and the lots.

Of course, this list is not exhaustive. We simply wanted to show that it was possible, for various processes, to identify the constraints influencing the manufactured product. However, we must keep in mind that there is a wide variety of constraints depending on the physical principle involved in the operation. Thus, it is impossible to give either a generic or a definite classification to guide the process selection. So, there is a stronger need to make all this information available during the design process. This requires identifying what kind of information is necessary for the designers, and at which time during the design process. Moreover, it is necessary to hold account of the constant evolution of the processes and to integrate it into the design tools so that designers do not design according to obsolete processes.

2 MEMS DESIGN TOOLS AND METHODOLOGIES

In order to be able to integrate process constraints in the design process, we were interested in the MEMS design methodologies and especially the way process constraints and capabilities can be integrated. Two types of methods seem to emerge: the first is design for manufacturability, a methodology

that considers manufacturability during the design process in order to design manufacturable MEMS. These methods already exist in the fields of electronics or traditional mechanics, and [5] proposes to adapt it to the design of manufacturable MEMS. DFM is an alternative to the traditional MEMS-product development cycle in which in particular "build and test" approach increases the design process and product costs. This method is also proclaimed by one of the renowned integrated specific MEMS design tools, CoventorWare, composed of four main products, which include ARCHITECT, ANALYSER and INTEGRATOR. We will be interested in the applications of the methods in those products, like those presented in [6].

The second method is based on the share of manufacturing knowledge using distributed web tools (that cannot be put in the category of integrated design tools) to help designers select the manufacturing processes and the material combinations.

2.1 Design For Manufacturability

DFM is well known as a design methodology that aims to reduce manufacturing times and costs [7]. In contrast, we will try to value the assistance provided by such a method in the crucial problem of process selection. Fundamental activities of MEMS development may be broadly divided into four overlapping phases, organized as shown in Figure 6.

Technical Specification Development. This is the phase where the needs of the customer are converted into engineering requirements and technical specifications, the starting points of the following phase. It is important that the customer requirements' document maintains the original intent of the customer and is not overly influenced by the perceptions of the engineering teams.

Conceptual Design Phase. This is the phase where designers develop and evaluate many design concepts simultaneously so as to offer enough choices for a successful product. For that, they create then use libraries of standard parametrized component elements that they can piece together to create more complex designs. Each element of the library is essentially an analytical or semi-analytical model that captures the behaviour of the element accurately over all possible displacements of the element. All the parameters of the element model are available to the designers as a variable to be defined and set. For instance, the non-linear beam-element model is the model of an Euler beam, where parameters such as length, thickness, width, as well as material properties such as the Young's modulus, Poisson's ratio, residual stress are all available as variables. As MEMS can sustain mechanical deformations in 3D space, each component model necessarily has 6 degrees of freedom. A schematic model assembled from parametrized library components immediately enables very rapid and accurate characterization of the behaviour of a specific conceptual design. One of the advantages of these phases is the ability of designers to design through process constraints. Indeed, parameters may be well defined within the tolerances of the specific manufacturing unit, and this influences the product-development

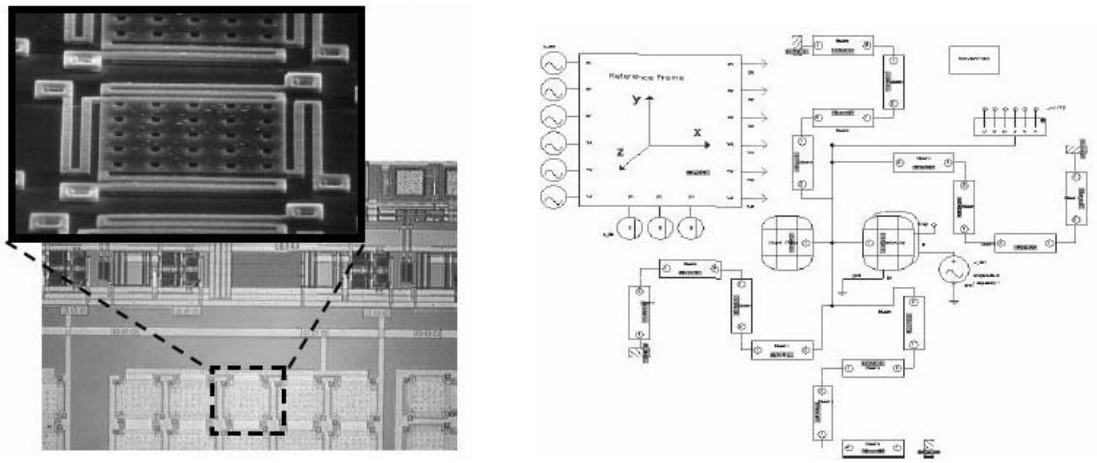

Fig. 7. *CMOS variable capacitor (left) and its schematic model*

process substantially, as only those designs that can be manufactured within the process are considered. Figure 7 shows an example of the conceptual design phase of a variable capacitor designed using ARCHITECT. We can see an image of the CMOS fabricated device (left) and the schematic model (bottom). Each "component" in the schematic model corresponds to a part of the CMOS fabricated device: for instance, the four folded suspension arms are each modelled with four connected parametrized beams.

Detailed Design Phase. During this phase a detailed engineering analysis of the selected design concepts is performed in order to provide additional details of the behaviour of the design or to study the effects not captured at the schematic level during the conceptual design phase. CoventorWare has an analysis tool, ANALYSER, composed of different bundles, which include for instance: finite-element methods (FEMs), for mechanics and general fluidics, boundary element methods (BEMs), for electrostatics and inductance, etc. All the ANALYSER bundles include, moreover, a MEMS-specific mesh generation. These details make it possible for the designers to optimize the product shape and to assess tolerance specifications in order to reduce the production costs. For instance, for a variable capacitor, an analysis performed in the detailed design phase allowed designers to calculate the distribution of the pull-in voltage in the function of the tolerances of the material properties (thickness, stress gradients, etc.) Then, INTEGRATOR reduces the detailed 3D analysis produced in ANALYZER to a reduced-order model that can supplement Coventor's extensive ARCHITECT library of parametrized MEMS components.

Manufacturing Phase. The manufacturing phase begins concurrently with the initiation of the design group's activities, with the aim of:

- identifying critical process characteristics, such as verticality or surface roughness
- identifying and evaluating existing processes, in order to chose between a standard process, a slightly modified standard process or a newly developed process.

This necessarily requires characterization of the processes' capability and the materials' properties: for instance, experiments are initiated so as to determine what kind of shape can be made, and with which processes and materials. Processes' capability and materials' properties information is integrated into the parametrized models used in the design phases.

It should be pointed out that some traditional guidelines of DFM (in the mechanical engineering field) clearly arise in the MEMS context:

- use of standard components,
- develop a modular design,
- design for ease of fabrication,
- avoid separate fasteners.

But some are completely out of scope:

- minimize assembly directions,
- design parts for multi-use.

This only tends to prove that the DFM method cannot be a simple mix of methodology available in both the mechanical and electronic worlds.

After all, we can concentrate on information and distinguish which information should be useful for designers at the conceptual and detailed design phases.

Conceptual Design Phase. At this level the designer needs

- geometrical information, in order to know if he is designing a manufacturable product, and if so, with which process.
- material information, to know which material can be deposited, selected, etched, etc.
- economic information, to help him to choose between two processes having the same performance.
- thermal information, to know if the manufacturing temperature of one schematic element will damage others.

One needs, moreover, to take into account the maximum of information simultaneously because independently this information has only little interest. For instance, it is possible to obtain a rounded wall using a wet etching process, but not in silicon, because of the anisotropic etching properties of this material (taking into account simultaneously the geometrical and material information).

Detailed design Phase. During this phase the designer needs information on the limits of the capabilities of the processes, because in this phase one optimizes the geometrical product characteristics to obtain the required behaviour while assessing the tolerance specifications in order to reduce the production costs. The designer needs, for instance, the minimum thickness or temperature of a deposited material, the best roughness obtained after etching, etc.

2.2 Sharing knowledge using web tools.

The following approach is a more oriented "process selection". Due to the typically unstable context of R&D, designers currently tend to conceive MEMS in terms of processes and materials in which they are familiar and may not consider a process and material combination that may have proven to be more economic. To solve this problem some tools have been developed to help designers select the "best" manufacturing processes and material combinations, based on the sharing of knowledge using the internet and web databases ([8] and [9]).

Processes and materials characteristics are stored in web databases. For instance, on the website www.mems-exchange.org for the silicon nitride PECVD process, one can find information like thickness (the amount of material added to a wafer), atmosphere (to which the substrate is exposed during processing), material (which can be deposited), microstructure, uniformity, wafer geometry, wafer material, wafer thickness, etc. (see Figure 8).

Designers build a manufacturing sequence using this information, and submit it to a specialized team that validate the project or propose the best sequence.

The WebMems-Mass tool also contains manufacturing and materials data, but proposes an algorithm to select processes and material combinations against econo-technical criteria. While running, WebMems-Mass generates a dialogue with the designer to inquire and acquire information about batch size, typical tolerances size, overall shape, cost requirements, etc. Then, the user is given real-time feedback regarding a plausible fabrication sequence. At each step of the design process the user is presented with an updated, ranked list of manufacturing and material possibilities.

Of course, those tools are not integrated MEMS design tools and only help designers select the right manufacturing process and material combination. But these tools shared on the internet are well adapted to a concurrent collaborative design by making it easier for designers from different disciplinary and manufacturing teams to communicate. Using libraries of standard components for the design of new products certainly restricts, a little more, the design state space, but increases the guarantee of designing a manufacturable product. Another advantage of shared web tools is their facility with being updated in order to be aware of manufacturing processes evolution. This seems to be the most efficient answer to the lack of availability with the boundary limits of the manufacturing process.

3 CONCLUSION

MEMS products are getting increasingly popular everyday. Though the industrial context is still research-and-development oriented, efforts are being made to move to a mass-production era.

To achieve this conversion, the concept of manufacturability must be considered. At the present time, manufacturability roughly seems to rely on a good

Silicon nitride PECVD	
Fab site	Commercial
Process characteristics:	
Thickness Amount of material added to a wafer	2.0 µm
Ambient Ambient to which substrate is exposed during processing	nitrogen, silane, ammonia
Material	silicon nitride
Microstructure	amorphous
Sides processed	either
Uniformity	-0.03 .. 0.03
Wafer diameter	150 mm
Equipment	Oxford Plasmalab PECVD System
Equipment characteristics:	
Batch sizes	150 mm: 1

Fig. 8. *Example of typical information available to the designer*

process choice. So we have had a special interest in presenting a sample of manufacturing processes derived from VLSI technologies that our community (mechanical manufacturing) is not familiar with. This has allowed us to propose some rough qualifiers to the information that designers can integrate.

We now have to concentrate on building the manufacturing sequence. Indeed, process selection is only part of the manufacturing issue, and manufacturability is also concerned with process compatibility.

Another aspect of the problem is that the manufacturing process can be based on various physical principles and the knowledge attached to them, even expressed under a constraint form this does not prove easy to understand. Consequently, further studies have to be made concerning the cognitive aspect of the knowledge sharing, as very different communities of experts are involved in such projects.

Finally, VLSI technologies are pushed to their limits to let the designers be more innovative (by introducing non-silicon materials, for example) but we must already think about the integration of innovative technologies in the current design process. This means the introduction of additional, different physical principles (micro-cutting, abrasives, etc.). This will increase the need for a unified classification of manufacturing constraints that would overcome the limits of disciplinary expertise.

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